ABSTRACT OF THE DISCLOSURE

A method of CMP planarizing a silicon dioxide layer on a silicon nitride in the semiconductor die is disclosed. A wafer has a plurality substantially identical semiconductor dies defined on the wafer. Each of the dies is separated from one another by a scribe line. A layer of silicon nitride is formed on the planar surface of the wafer where the silicon nitride has a top surface which is substantially parallel to the planar surface. A layer of silicon dioxide is deposited on the top surface with the silicon dioxide varying in height above the top surface. A mask is formed across the wafer, including on the scribe line, where the mask has a plurality of locations with each location having a differing density of gap-to-pillar ratio, which is proportional to the height of the silicon dioxide above the top surface. The silicon dioxide is anisotropically etched through each gap of the mask across the entire wafer where each gap is etched by the same amount in the height direction. CMP is then used to planarize the silicon dioxide to the top surface of the silicon nitride across the entire wafer.